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Abstract
The discrete wavelet transform(DWT) is useful in many different fields, including signal analysis, signal compression, pattern recognition, and numerical analysis, especially in image/video compression. The DWT decomposes signals into different frequency bands, and performs a multiresolution analysis.

Because the traditional DWT is composed of filters, the VLSI implementation complexity is very high. In 1996, lifting-based DWT is proposed. The advantages of the lifting-based DWT are lower implementation complexity and less hardware resources. The lifting-based DWT is also used in the newest image standard - JPEG-2000.

In this paper, we propose two 2-D DWT architectures. In the first part, we present a salable architecture for 2-dimensional lifting-based DWT. Because of downsampling of the DWT, the hardware utilization is very low. In order to solve the problem, we propose a pipelined and merged architecture, which combines the horizontal and vertical DWT together. We also add some control circuits to make the architecture suitable for different decomposition levels. In the second part, we present an architecture for 2-D 3-level lifting-based DWT. We propose two different methods for row and column transforming to reduce the storage size of the architecture. The proposed architecture computes 2-D 3-level DWT coefficients concurrently, and achieves higher hardware utilization.

The proposed VLSI architectures are described in Verilog HDL, and synthesized by the Synopsys' Design Compiler. Finally, the layout of the design is generated automatically by the Avant! Apollo Layout Tools in a 0.35μm 1P4M CMOS technology. The chip area is about 2055 x 2055 μm2.
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